

#7/B  
3/7/3  
Sunder

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Stephen W. Russell  
Serial No.: 09/938,260  
Filing Date: 08/23/2001  
Title: IMPROVED DIELECTRIC LAYER LINER FOR AN INTEGRATED CIRCUIT STRUCTURE

Art Unit: 2815  
Examiner: Fenty, J. A.  
Docket No.: TI-25084

Amendment under 37 CFR 1.111

Assistant Commissioner of Patents  
Washington, DC 20231

FAX RECEIVED

MAR 4 2003

TECHNOLOGY CENTER 2800

Dear Sir:

The following amendments and remarks are offered in response to the Examiner's Office Action dated 11/04/2002. They are respectfully submitted as a full and complete response to that Action.

Please amend the above-referenced application as follows:

In the Claims:

Replace claim 1 with the following claim:

- B'
1. (amended) An integrated circuit structure, comprising:  
a plurality of solid state electronic devices;  
a plurality of conductive elements electrically coupling the electronic devices;  
a dielectric layer positioned between two or more of the conductive elements; and

To: Technology Center 2800  
Facsimile Number: 703-872-9318

Total Pages Sent 10

From: Jacqueline J. Garner  
Texas Instruments Incorporated  
Facsimile: 972-917-4418  
Phone: 214-532-9348

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Stephen W. Russell

Art Unit: 2815

Serial No.: 09/938,260

Examiner: Fenty, J. A.

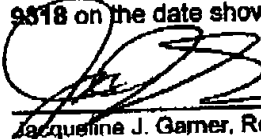
Filing Date: 08/23/2001

Docket No.: TI-25084

Title: IMPROVED DIELECTRIC LAYER LINER FOR AN INTEGRATED  
CIRCUIT STRUCTURE

**CERTIFICATION OF FACSIMILE TRANSMISSION**

I hereby certify that the following papers are being transmitted by  
facsimile to the U.S. Patent and Trademark Office at 703-872-  
9318 on the date shown below:

  
Jacqueline J. Garner, Reg. No. 36,144

March 4, 2003  
Date

**FAX RECEIVED**

MAR 4 2003

TECHNOLOGY CENTER 2800

**FACSIMILE COVER SHEET**

<input checked="" type="checkbox"/> FACSIMILE COVER SHEET	<input checked="" type="checkbox"/> AMENDMENT (5 Pages)
<input type="checkbox"/> NEW APPLICATION	<input checked="" type="checkbox"/> EOT 1 mth (3 Pages)
<input type="checkbox"/> DECLARATION (# Pages)	<input type="checkbox"/> NOTICE OF APPEAL (# Pages)
<input type="checkbox"/> ASSIGNMENT (# Pages)	<input type="checkbox"/> APPEAL (# Pages)
<input type="checkbox"/> FORMAL DRAWINGS	<input type="checkbox"/> ISSUE FEE (# Pages)
<input type="checkbox"/> INFORMAL DRAWINGS	<input type="checkbox"/> REPLY BRIEF (IN TRIPLICATE) (# Pages)
<input type="checkbox"/> CONTINUATION APP'N (# Pages)	
<input type="checkbox"/> DIVISIONAL APP'N	
<b>NAME OF INVENTOR(S):</b> Russell	
<b>TITLE OF INVENTION:</b> Improved Dielectric Layer Liner	
<b>TI FILE NO.:</b> TI-25084	<b>DEPOSIT ACCT. NO.:</b> 20-0868
<b>FAXED:</b> March 4, 2003 <b>DUE:</b> 2/4/2003 <b>ATTY/SEC'Y:</b> JJG	
<b>RECEIPT DATE &amp; SERIAL NO.:</b> <b>Serial No.:</b> 09/938,260 <b>Filing Date:</b> 08/23/2001	

This facsimile is intended only for the use of the address named and contains legally privileged and/or confidential information. If you are not the intended recipient of this telecopy, you are hereby notified that any dissemination, distribution, copying or use of this communication is strictly prohibited. Applicable privileges are not waived by virtue of the document having been transmitted by Facsimile. Any misdirected facsimiles should be returned to the sender by mail at the address indicated on this cover sheet.

Texas Instruments Incorporated  
PO Box 655474, M/S 3899  
Dallas, TX 75074